WHAT IS CLAIMED IS:

1. An apparatus for controlling a physical layer interface of a network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program;

a random access memory capable of storing a downloadable software control program; and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said embedded control program to thereby control said physical layer interface.

2. The apparatus as set forth in Claim 1 wherein said ROM is an internal ROM in said microcontroller.

3. The apparatus as set forth in Claim 1 wherein said RAM is an internal RAM in said microcontroller.

4. The apparatus as set forth in Claim 1 wherein said ROM is an external ROM coupled to said microcontroller.

5. The apparatus as set forth in Claim 1 wherein said RAM is an external RAM coupled to said microcontroller.

6. The apparatus as set forth in Claim 1 wherein said microcontroller downloads said downloadable software control program from said external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

7. The apparatus as set forth in Claim 6 wherein said microcontroller downloads said downloadable software control program via a medium access control (MAC) layer interface coupling said external processing system and said physical layer interface.

8. The apparatus as set forth in Claim 1 wherein said microcontroller further comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address in said RAM in a first one of said plurality of control registers.

9. A processing system comprising:

a data processor;

a hard disk drive capable of storing thereon a network interface card (NIC) configuration file containing a downloadable software control program; and

a network interface card for coupling said processing system to a data network, said network interface card comprising:

an apparatus for controlling a physical layer interface of said network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program;

a random access memory capable of storing a downloadable software control program; and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said

embedded control program to thereby control said physical layer interface.

10. The processing system as set forth in Claim 9 wherein said ROM is an internal ROM in said microcontroller.

11. The processing system as set forth in Claim 9 wherein said RAM is an internal RAM in said microcontroller.

12. The processing system as set forth in Claim 9 wherein said ROM is an external ROM coupled to said microcontroller.

13. The processing system as set forth in Claim 9 wherein said RAM is an external RAM coupled to said microcontroller.

14. The processing system as set forth in Claim 9 wherein said microcontroller downloads said downloadable software control program from said external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

15. The processing system as set forth in Claim 14 wherein said microcontroller downloads said downloadable software control program via a medium access control (MAC) layer interface coupling said external processing system and said physical layer interface.

16. The processing system as set forth in Claim 9 wherein said microcontroller further comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address in said RAM in a first one of said plurality of control registers.

17. For use in a network interface card having a physical layer interface controllable by a microcontroller embedded therein, a method of operating the microcontroller comprising the steps of:

in a first operating mode, executing an embedded control program stored in a read only memory (ROM) coupled to the microcontroller to thereby control the physical layer interface;

in a second operating mode, downloading a software control program from an external processing system and storing the software control program in a random access memory (RAM) coupled to the microcontroller and, in response to the step of downloading the software control program, executing the software control program in place of the embedded control program to thereby control the physical layer interface.

18. The method as set forth in Claim 17 wherein the ROM is an internal ROM in the microcontroller.

19. The method as set forth in Claim 17 wherein the RAM is an internal RAM in the microcontroller.

20. The method as set forth in Claim 17 wherein the ROM is an external ROM coupled to the microcontroller.

21. The method as set forth in Claim 17 wherein the RAM is an external RAM coupled to the microcontroller.

22. The method as set forth in Claim 17 wherein the step of downloading comprises the step of downloading the software control program from the external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

23. The method as set forth in Claim 22 wherein the step of downloading comprises the step of downloading the software control program via a medium access control (MAC) layer interface coupling the external processing system and the physical layer interface.